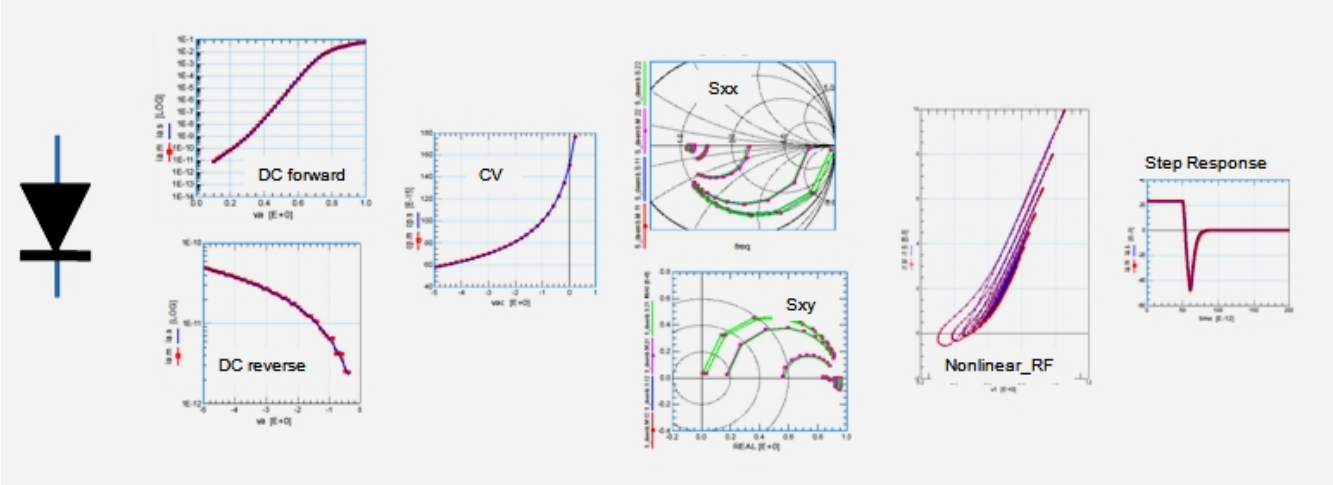
DIODE MODELING TUTORIAL

From DC → CV → S-Parameters → Nonlinear-RF → Time Domain



Keywords:
Diode Spice Model, DC Forward and Reverse Modeling, Space Charge and Diffusion Charge Modeling, Nonlinear-RF Modeling and Model Inspection

Contents:

Publication Status: 26.April 2023

SisConsult
Ingenieurbüro - Engineering Office
Dr.-Ing. Franz Sischka
Consulting Services for Electronic Device Measurements, Data Verification and Modeling
www.SisConsult.de

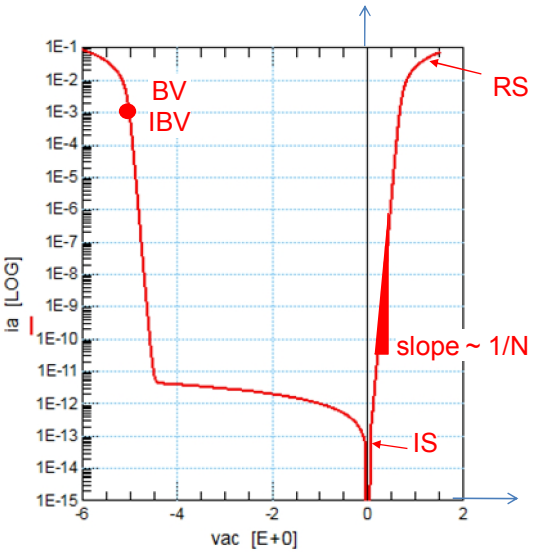
Introduction

Why a Tutorial about Diode Modeling ?

- its equations are easy to understand
- can be found as part of bipolar, MOS and MESFET models
- a good training to better understand other non-linear models

SisConsult 3

The Basic Spice Diode Model



SPICE Version 2G User's Guide

(10 Aug 1981)

A.Vladimirescu, Kaihe Zhang,
A.R.Newton, D.O.Pederson, A.Sangiovanni-Vincentelli

Department of Electrical Engineering and Computer Sciences
University of California
Berkeley, Ca., 94720

7.6. Diode Model

The dc characteristics of the diode are determined by the parameters IS and N. An ohmic resistance, RS, is included. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance which is determined by the parameters CJO, VJ, and M. The temperature dependence of the saturation current is defined by the parameters EG, the energy and XTI, the saturation current temperature exponent. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV (both of which are positive numbers).

	name	parameter	units	default	example	area
1	IS	saturation current	A	1.0E-14	1.0E-14	*
2	RS	ohmic resistance	Ohm	0	10	*
3	N	emission coefficient	-	1	1.0	
4	TT	transit-time	sec	0	0.1Ns	
5	CJO	zero-bias junction capacitance	F	0	2PF	*
6	VJ	junction potential	V	1	0.6	
7	M	grading coefficient	-	0.5	0.5	
8	EG	activation energy	eV	1.11	1.11 Si 0.69 Sbd 0.67 Ge	
9	XTI	saturation-current temp. exp	-	3.0	3.0 jn 2.0 Sbd	
10	KF	flicker noise coefficient	-	0		
11	AF	flicker noise exponent	-	1		
12	FC	coefficient for forward-bias depletion capacitance formula	-	0.5		
13	BV	reverse breakdown voltage	V	infinite	40.0	
14	IBV	current at breakdown voltage	A	1.0E-3		

- a good and robust 1st order model
- although too simplistic in many applications, it can be cascaded for better fitting the reality

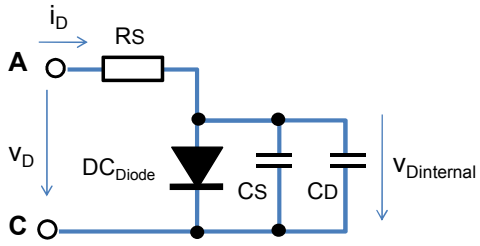
SisConsult -4-

Effects not covered by the standard SPICE diode model are:

- recombination effect (low forward DC bias)
- reverse off-state current between 0V and breakdown voltage

  Note: In practice, this is never simply IS

The Basic Spice Diode Model in Details



RS Series resistor
DC_{Diode} the non-linear DC current characteristic
CS Space charge capacitance, the main capacitive effect
CD Diffusion capacitance, the transit time effect

The model equations:

$$i_{Dfwd} = I_S \left[\exp\left(\frac{v_{Dinternal}}{N \cdot vt}\right) - 1\right] + v_{Dinternal} \cdot Gmin$$

$$i_{Drev} = I_S \left[\exp\left(-\frac{v_D + B_{Veff}}{vt}\right) - 1\right]$$

$$C_s = C_{JO} \Big/ \left(1 - \frac{v_D}{V_J}\right)^M$$

$$C_D = T_T * g_D = T_T * \frac{1}{N \cdot vt} \cdot i_D$$

IS Saturation Current (leakage current, typical fA)
N Emission Coefficient (ideal diode: N=1)
vt Temperature Voltage 27mV at 25°C
vt = k*T/q = 8.6171 E-5 * (T /°C + 273.15)
Gmin Simulation Convergence Aid ($Gmin_{default}$=1E-12)

BV Breakdown Voltage in DC Reverse Biasing
IBV Current at Breakdown Voltage
Note: Spice calculates BVeff from parameters BV and IBV)

CJO Space Charge Capacitance at vD = 0V
VJ Built-in Potential or Pole Voltage (typ. 0,7V)
M Junction Exp. Factor, the Slope of the CV Plot

TT transit time

SiConsult

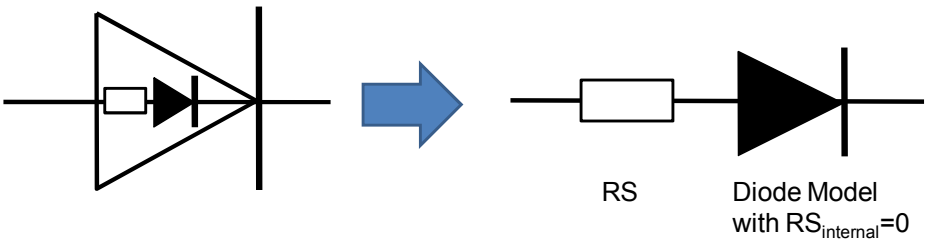
5

The SPICE Diode Model Parameter List:

param.	description	units	default	example.
RS	ohmic resistance	Ohm	0	10
IS	saturation current	A	1.0E-14	1.0E-14
N	emission coeff.	-	1	1
BV	rev. breakdown volt.	V	inf.	40
IBV	current at BV	A	1.E-3	
CJO	zero bias junct. cap.	F	0	2.0E-12
VJ	junction potential	V	1	0.6
M	diffusion grading coeff.	-	0.5	0.5
FC	CJ lin. extens.coeff.	-	0.5	0.5
TT	transit time	sec	0	1E-10
EG	activation energy	eV	1.11 for Si 0.67 for Ge	
XTI	sat. current temp.exp.	-	3.0	3
KF	flicker noise coefficient	-	0	
AF	flicker noise exponent	-	1	
TNOM	modeling temp.	'C	27	

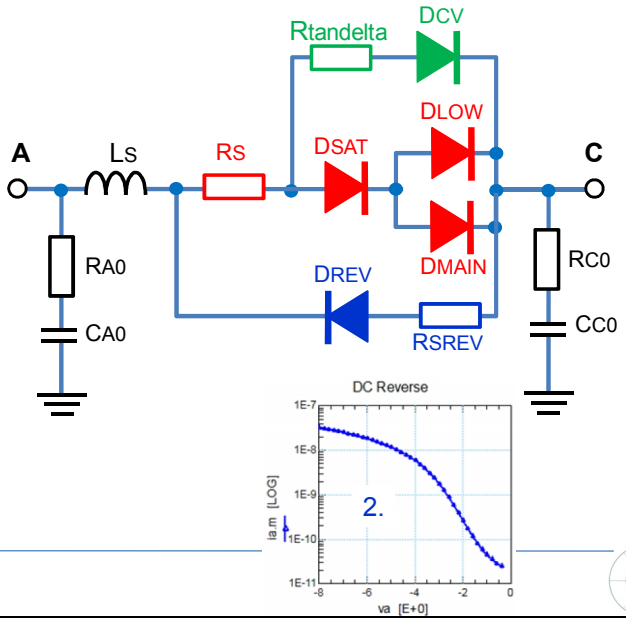
Based on (*verified*) measurements,
we will now develop an accurate diode model
by cascading the basic diode model into a sub-circuit.

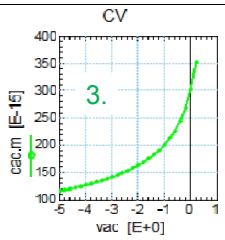
To keep things separated,
we will not use the model-internal resistor RS,
but will use a separate resistor model instead.

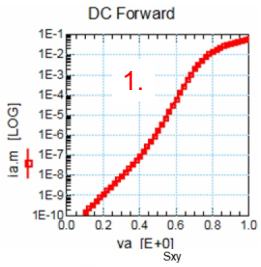


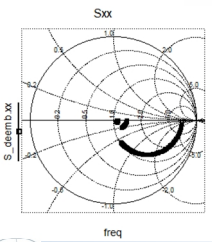
6

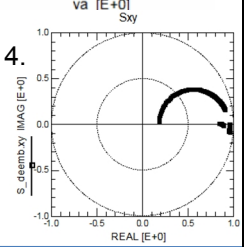
A Quick Preview of the Modeling Steps











7

This slide gives a quick preview about what will be covered in this tutorial.

Back to Top

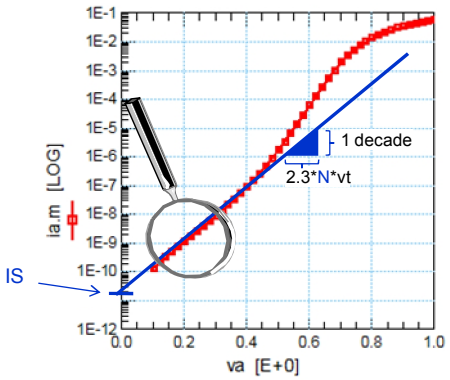
DC Forward Modeling

Outline

- Introduction
- **Modeling Steps**
  - **DC Forward**
  - DC Reverse
  - CV Modeling
  - S-Parameter
- Nonlinear-RF Inspection
- Time-Domain Inspection
- Modeling Result

SisConsult 8

Following best practice, the modeling begins with the lowest DC bias



DLOW

$$i_D = IS\left(\exp\left(\frac{v_D}{N \cdot vt}\right) - 1\right)$$

$$\sim IS \cdot \exp\left(\frac{v_D}{N \cdot vt}\right)$$

LOG_{10} converted

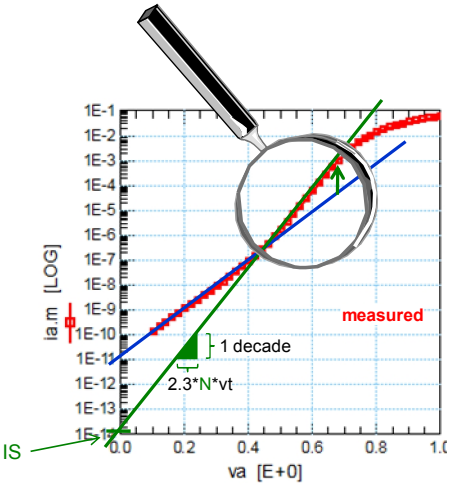
$$LOG(i_D) = LOG(IS) + \frac{v_D}{N \cdot vt} \cdot LOG(e)$$

$$= LOG(IS) + 1/(2.3 \cdot N \cdot vt) \cdot v_D$$

$$y = y0 + m \cdot x$$

SisConsult 9

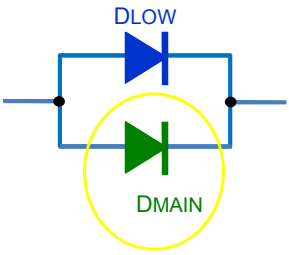
DC Forward Modeling Towards Higher Bias



For higher bias voltages,
the so far applied low-bias diode DLO
does not predict enough current:

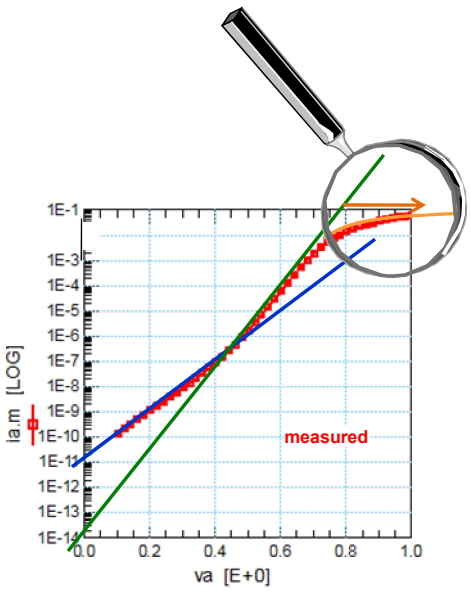
The measured current (*at the same bias voltage*)
- is considerably bigger

- The measured current trace is again linear
  -> another diode (DMAIN), in parallel to DLO



SisConsult

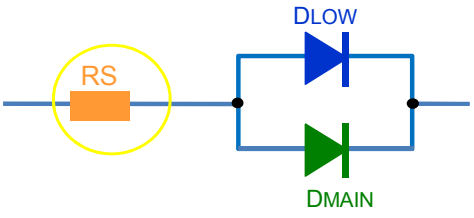
DC Forward Modeling into the Ohmic Diode Behavior



Beyond diode threshold,
going into the ohmic range,
there is an additional voltage drop
(*at the same bias current*)

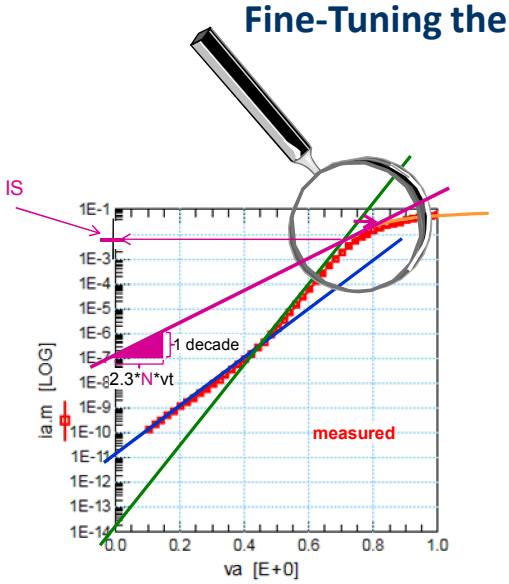
- In a lin/lin plot,
  the measured current trace is linear.
  Therefore, we add a

-> series resistor RS



SisConsult

DC Forward Modeling:
Fine-Tuning the Transition to the Ohmic Range

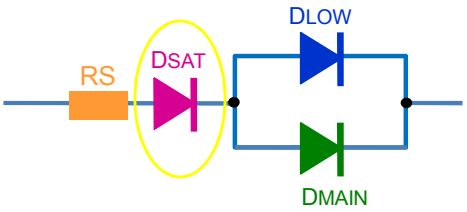


Best-Practice Modeling Step:

In order to improve the fitting in the curve's transition range to RS we

- add a series diode DSAT

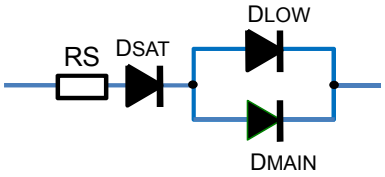
which provides an additional voltage drop at the same current value.

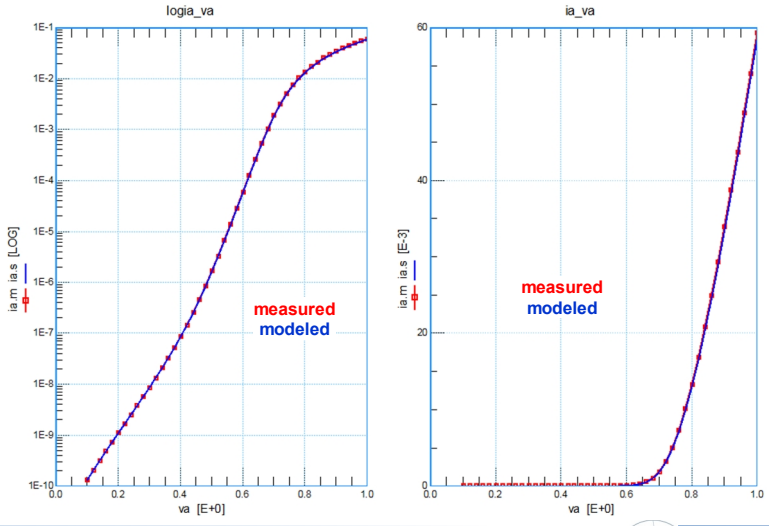


sConsult

12

The DC Forward Model Fit





sConsult

12

Back to Top

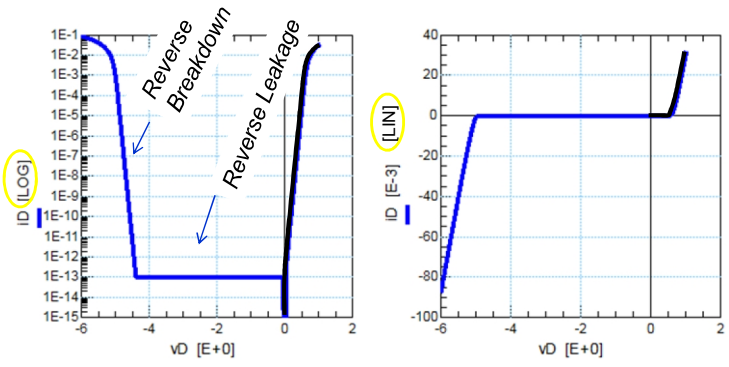
DC Reverse Modeling

Outline

- Introduction
- **Modeling Steps**
  - DC Forward
  - **DC Reverse**
  - CV Modeling
  - S-Parameter
- Nonlinear-RF Inspection
- Time-Domain Inspection
- Modeling Result

SisConsult 13

The Reverse Spice Diode Model



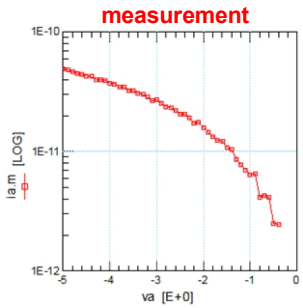
Reverse Spice Diode Model Limitations:

Constant Rev. Leakage Current: IS

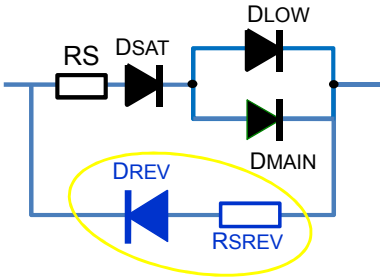
Rev. Breakdown slope is fixed: $\frac{\partial i_D}{\partial v_D} = \frac{1\ \text{decade}}{2.3 \cdot vt}$

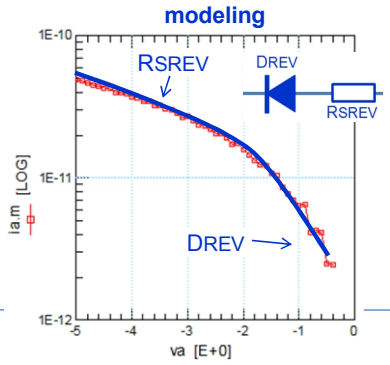
SisConsult -14-

Enhancing The Model to Fit the Reverse Measurements



To model the reverse leakage more accurately,
we add a reverse diode and resistor
to the modeling sub-circuit:

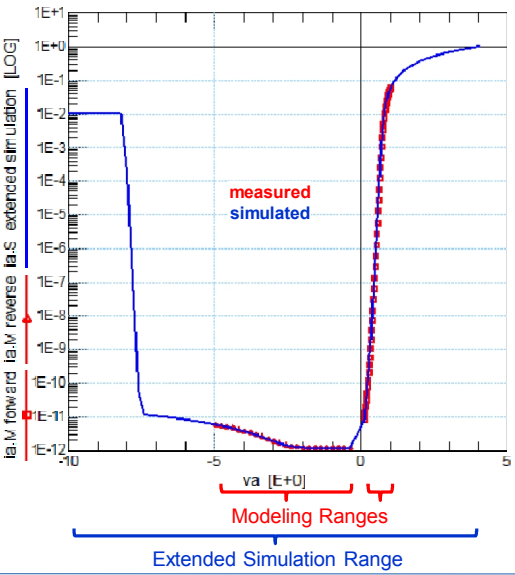




-15-

After the DC Modeling ---

Verification of the DC Model Robustness



After the DC modeling is done,
it is very important to verify
the model stability:

- apply larger bias stimulations
- apply large simulation temperatures

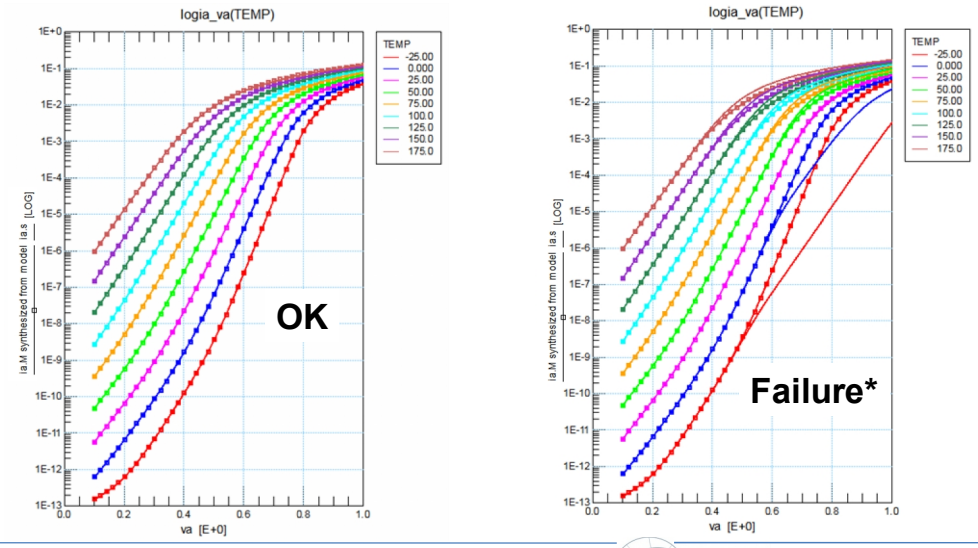
The goal is to check
if the model *explodes* or not.

-16-

Background: in large-signal RF and in time-domain simulations, the simulator will apply biases which may exceed the modeling range, in order to find a solution for the given modeling problem. If the model would explode, the simulator would go into error state.

Verifying DC Model Consistency vs. Temperature

Simulation of different device temperatures based on modeling at TEMP=27'C



* here: due to a wrong temperature-dependence setting of DSAT

SiConsult

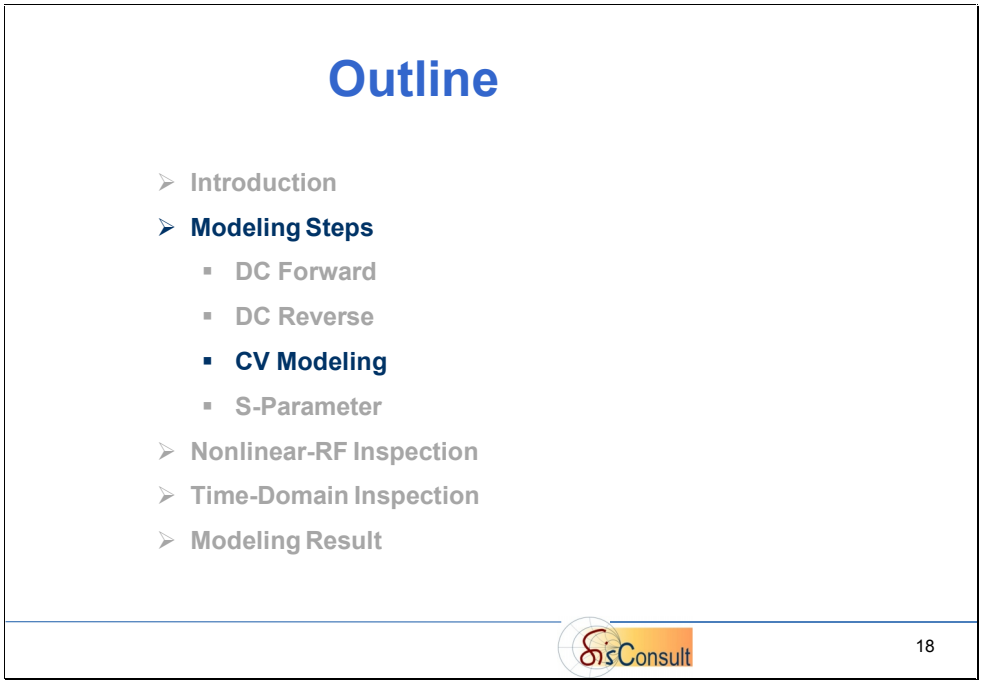
-17-

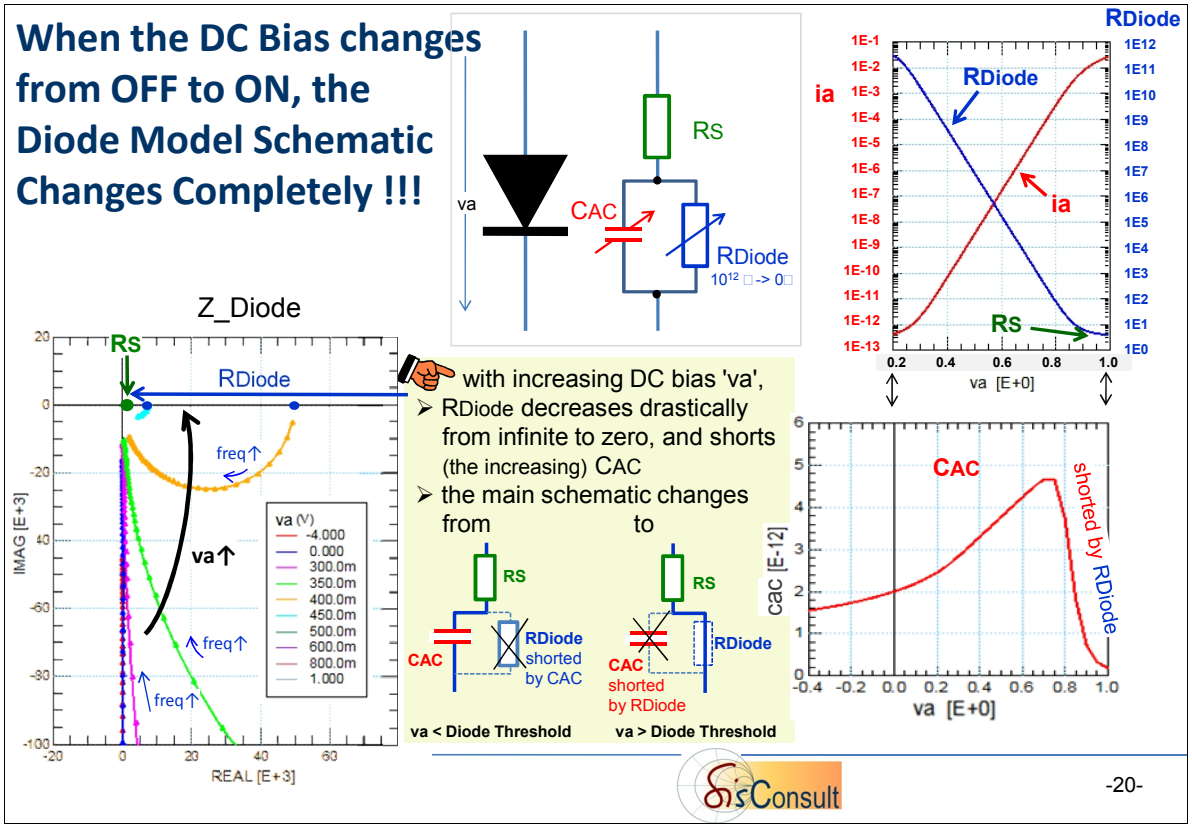
To verify the so far obtained DC model, a prediction simulation of the device behavior at different temperatures is applied to check for abnormalities:
-> expected is a smooth increase of the current with temperature.

The failure shown above on the right is due to an overlay of the wrong temperature-dependence of DSAT.
By switching-off the temperature effect of this 'fitting diode', we obtain the correct behavior as shown on the left.

Back to Top

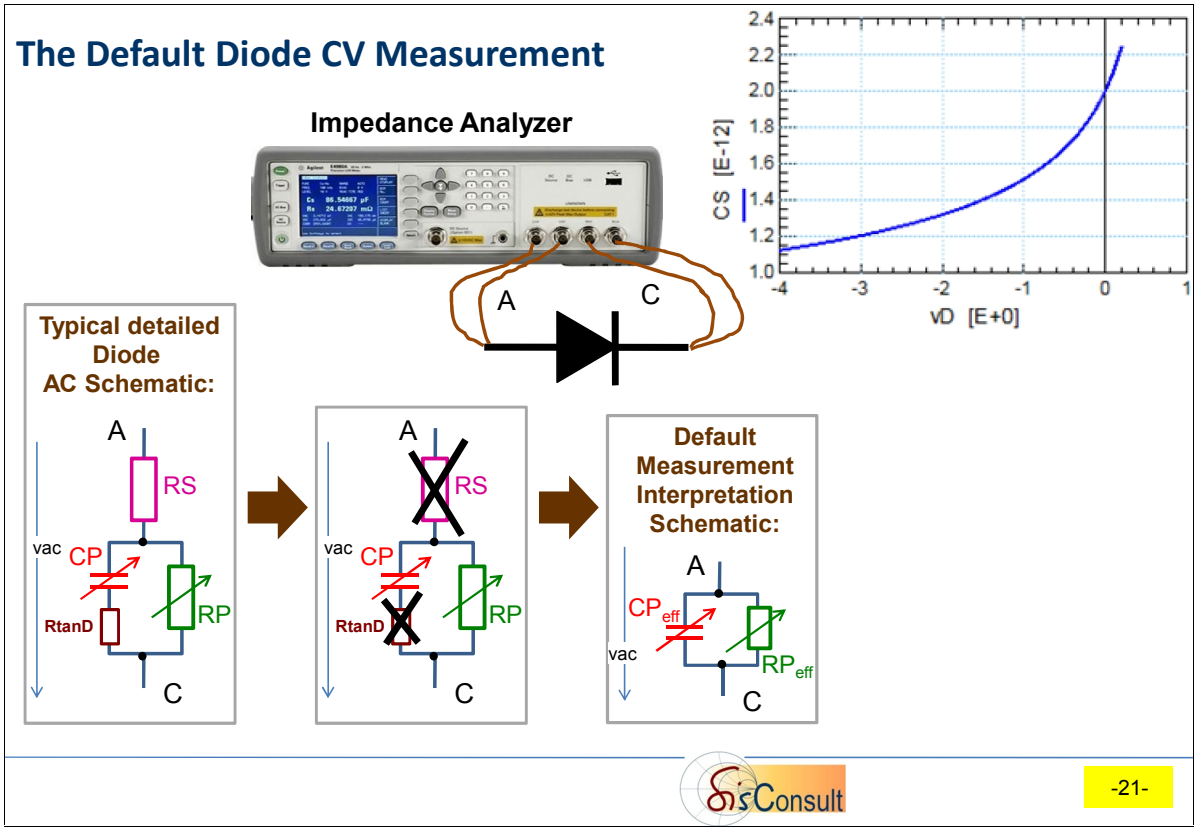
CV Modeling





An interesting effect of the bias-dependence of the diode schematic is the change from a mainly series schematic (CAC & RS) for negative DC bias, via a mainly parallel schematic (CAC & RDiode) around threshold, to RS alone at max. positive DC bias (when RDiode is shorting the capacitance CAC).

Note: In the plot Z_Diode, the end point of all traces for all DC biasings and for infinite frequency is Z=RS.



For the CV measurement, an Impedance Analyzer is applied. The stimulation frequency is usually set to 1MHz, the RF signal level is kept at its default value, and the DC bias is swept.

Furthermore, most modeling engineers keep the instrument's default measurement setting what means that the measured impedance, independently how complex its Spice schematic might be, is interpreted and displayed as a capacitance (CP) *in parallel* with a resistor (RP). And usually, only the capacitance measurement result is applied for device modeling, as shown above on the upper right.

However, for a diode, with its bias-dependent impedance change from OFF to ON, this default measurement neglects the *series* resistor RS and neglects also the usually present capacitor loss, represented by a resistor RtanD *in series* with the capacitor (see above). And this simplification explains why the measured capacitance and resistor curves may become frequency-dependent. Modeling engineers then usually apply lower measurement frequencies to avoid this.

A best-practice recommendation is, to measure the impedance *without* any simplifications. Then, inspect the Impedance Plot trace and identify the underlying Spice schematic. This will enable to identify the effect of RtanD, and consequently, a more precise Spice schematic to be modeled.

Notices:

- **RF Signal Power Level:**

It is strongly recommended to control the applied RF signal power, and not to simply keep the instrument's default value which is often too big, especially for CV curves with a big change in slope. In such a case, a too big AC signal may change the DC biasing: the measured capacitance value is the mean value of the capacitances *around* the bias point.

The procedure to identify the maximum applicable RF signal level is simple:

Start with a low AC signal of e.g. 10mV, and perform a measurement. Then re-perform the measurement, but with an increased RF signal value. Compare with the previous measurement result. If both are the same, you can further increase the signal level (in order to obtain a better signal-to-

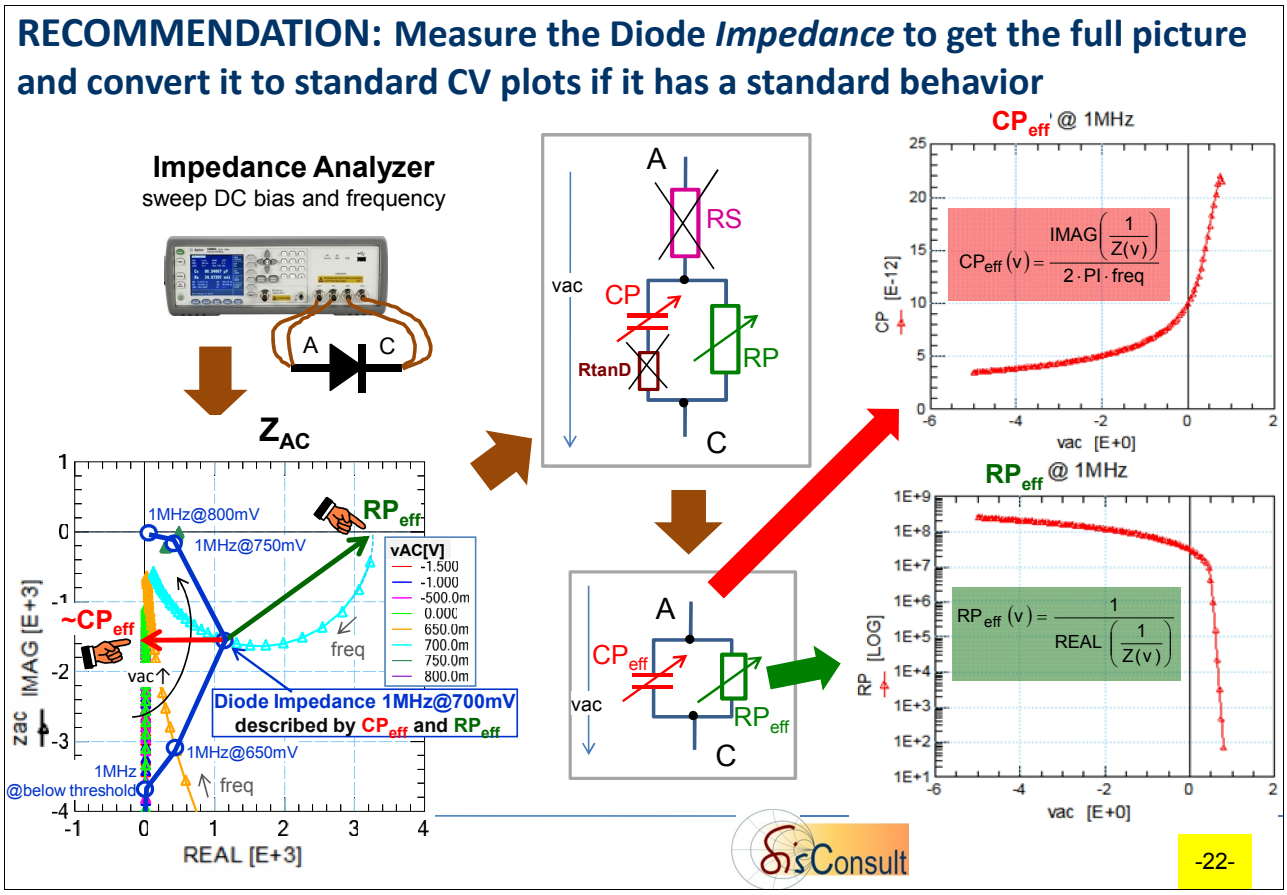
noise ratio) until you see a change in the measurement result. Then, keep the signal level which did not yet affect the measurement.

➢ **What to do with device pins not connected to the measurement**

If your diode also has a 3rd connection (e.g. the wafer bulk), connect it to the shielding of the impedance analyzer's BNC connectors. Due to the measurement principle of today's impedance analyzers (balancing bridge), stray capacitors from Anode or Cathode to Bulk will not be included by the measurement (i.e. added to the desired Anode-Cathode-Capacitance).

A recommendation for experts:

For a precise Spice model of a diode, it is recommended to measure the diode impedance, with the frequency as the first sweep, and DC bias as the second, and to display the complex impedance in a Real/Imaginary Plot, as shown below. From the impedance traces, a detailed Spice model can be derived, which is often much more complex than just a single, bias-dependent capacitance.



From such an impedance measurement, a simple conversion of the real and the imaginary part of the bias-swept (and default-1MHz single-frequency) diode impedance Z into 'CP_{eff} parallel to RP_{eff}' can be applied by the modeling program (see the formulas above) and we are back with the conventional CV modeling.

But with the advantage

- that we have a better picture of the real diode impedance characteristic,
- and that we have impedance measurements available if a more complex modeling might be required later.

... coming back to the CV Modeling:

The Space Charge Capacitance Modeling Formula

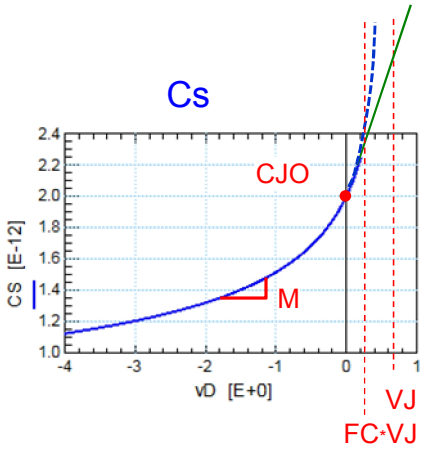
For $v_D < F_C * V_J$:

$$C_s(v_D) = \frac{C_{JO}}{\left(1 - \frac{v_D}{V_J}\right)^M}$$

and else (to avoid the pole at $v_D = V_J$), a linear continuation :

$$C_s(v_D) = \frac{C_{JO}}{(1-F_C)^{(1+M)}} * \left[1 - F_C * (1+M) + M * \frac{v_D}{V_J}\right]$$

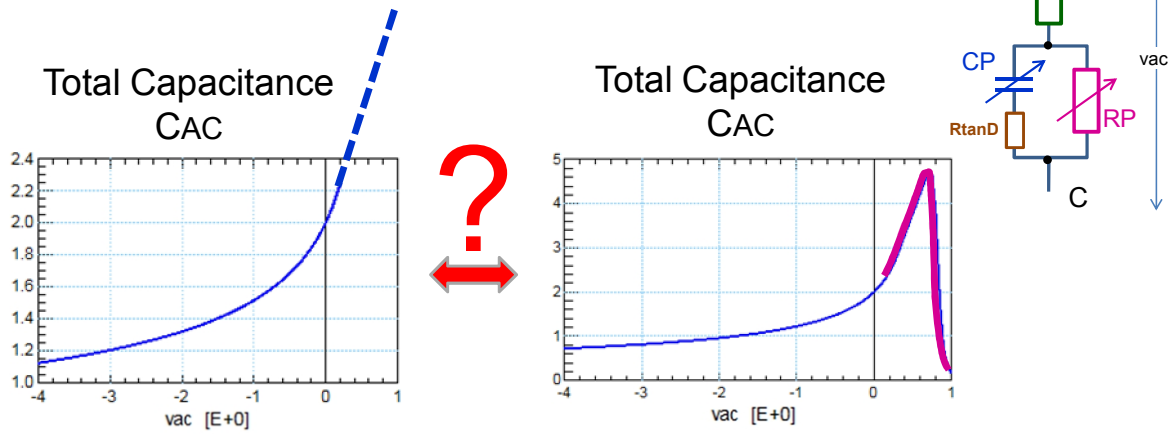
with $0 < F_C < 0.99$



SisConsult 23

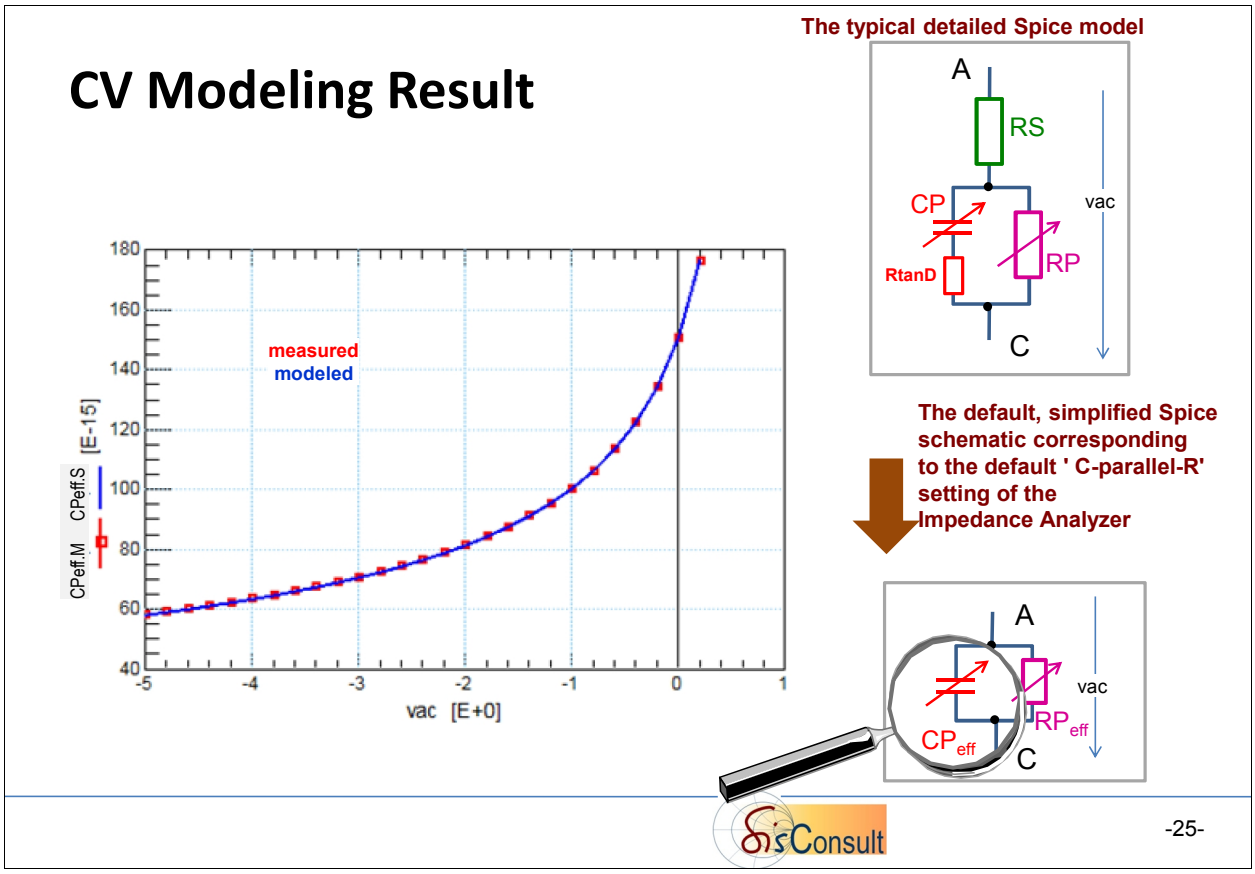
From the CV-plot, the Spice parameter CJO is directly the y-intercept, M is the slope in reverse DC bias, VJ the 'explosion point at positive bias, and FC*VJ the linear continuation of the Spice model

As a Foot Note:
About the Continuation of the Diode CV Model Curve into positive DC Bias



- Physically, the 'explosion' effect of the model equation for vac -> DC ON state is cancelled by the parallel resistor RP which becomes a short.
- Mathematically, however, and important for the performance of a simulator, the capacitance 'explosion' needs to be limited in order to avoid convergence problems.

SisConsult -24-



Back to Top

S-Parameter Modeling

Outline

- Introduction
- **Modeling Steps**
  - DC Forward
  - DC Reverse
  - CV Modeling
  - **S-Parameter**
- Nonlinear-RF Inspection
- Time-Domain Inspection
- Modeling Result

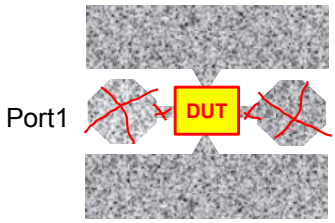
SiConsult 25

Important Note:

Measuring and Using S-Parameters for Modeling

before performing device modeling of S-Parameters, they have to be de-embedded carefully from possible overlaying connection and contact pads influences.

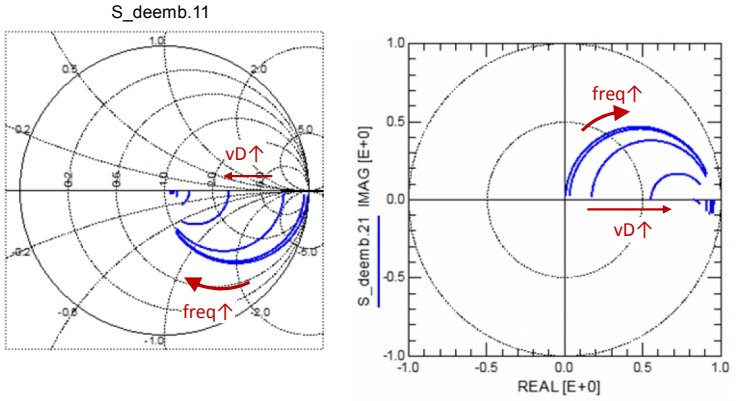
Only de-embedded S-Parameters with a verified de-embedding procedure shall be used.



SiConsult 26

S-Parameter Modeling

QUIZ:
which trace represents neg. DC bias, and which positive ?

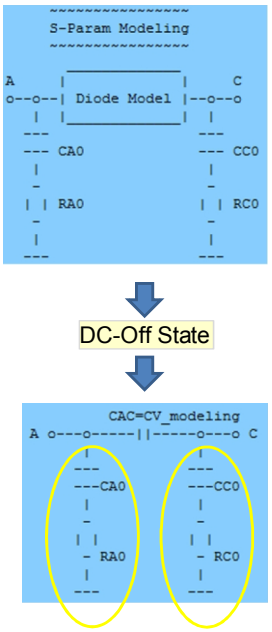


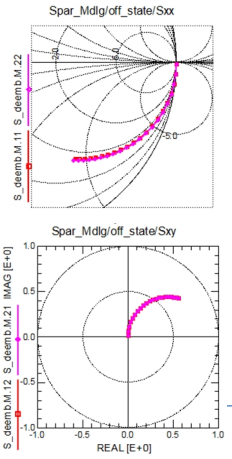
- the low-frequency starting points are determined by the DC
- the traces vs. frequency are determined by the capacitances
- the virtual end points (freq →∞) represent the model schematic with shorting capacitances

S-Parameter DC-OFF Modeling

DC-Off Spar Modeling: vD=-2V

Due to the CV Impedance measurement and modeling principle, the Anode-Cathode Capacitance CAC has been measured and modeled *without being overlaid* by the parasitic Anode-Ground and Cathode-Ground parasitics.





Using S-Parameters,
they become now visible, and will be modeled as capacitances (CA0, CC0) with tan-delta losses (RA0, RC0).

How to obtain the component values vs. freq:

~~~~~~

1. Transform the de-embedded and verified S-parameters to Y-parameters
2. calculate Admittances of PI Schematic:

```
Yxy = 0.5 * (Y.12+Y.21)
Y10 = Y.11+Yxy
Y20 = Y.22+Yxy
Y12 = -Yxy
```

3. convert to Impedances

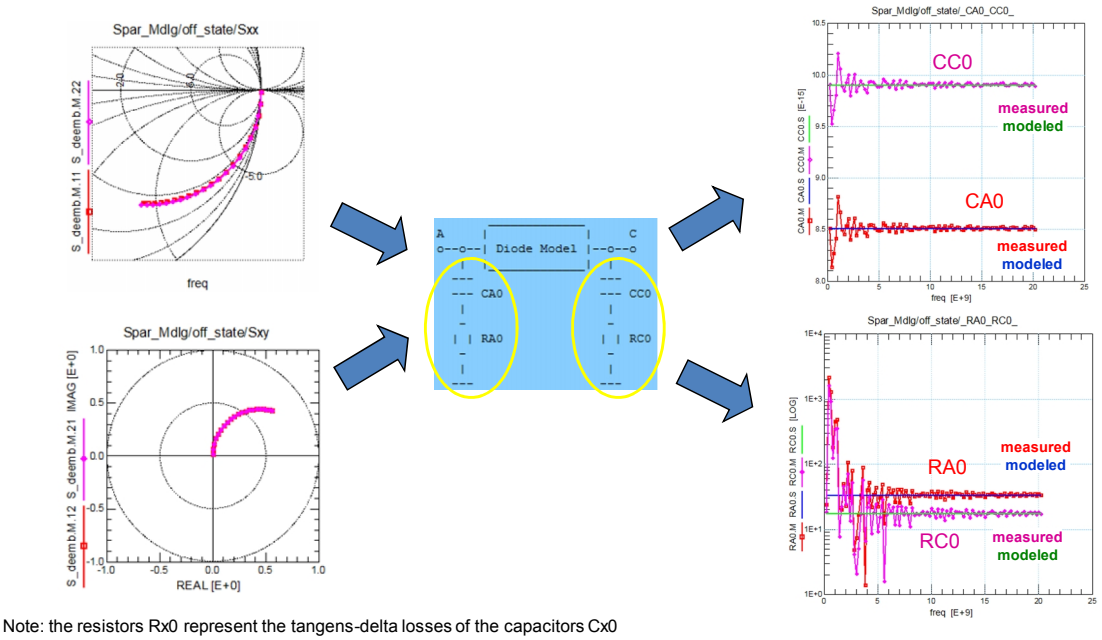
```
Z10 = 1/Y10
Z20 = 1/Y20
Z12 = 1/Y12
```

4. calculate PI Schematic elements

```
CA0 = -1/(IMAG(Z10)*2PI*f)
RA0 =  REAL(Z10)
CC0 = -1/(IMAG(Z20)*2PI*f)
RC0 =  REAL(Z20)
CAC = -1/(IMAG(Z12)*2PI*f)
RAC =  REAL(Z12)
```
~~~~~~

Fitting the Parasitic Capacitances

DC-Off Spar Modeling: vD=-2V



Note: the resistors Rx0 represent the tangens-delta losses of the capacitors Cx0

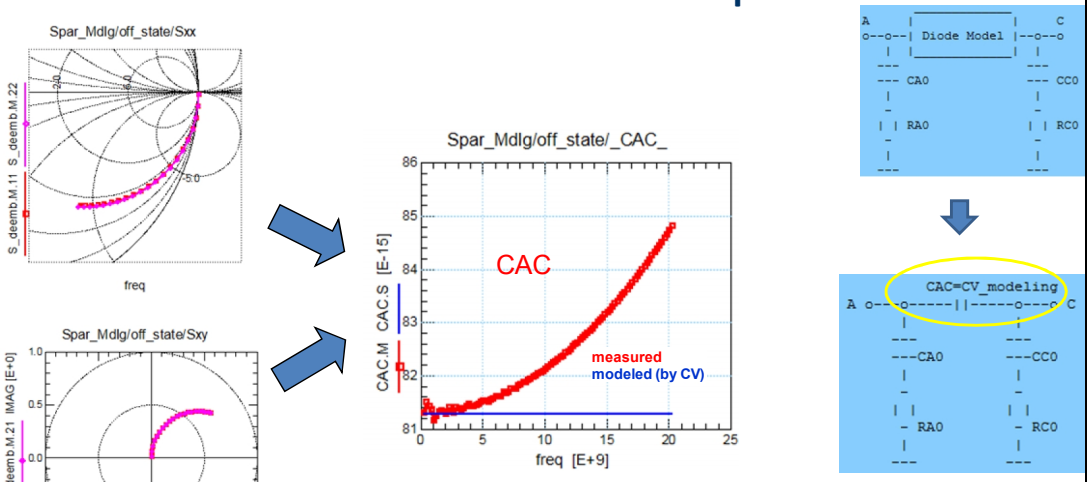
SisConsult

-29-

A note about the traces of Sxx:
-> If there was no parasitic CA0 nor CC0 at all, the traces of Sxx in the Smith Chart would start at the very right, at infinite Ohm (as it does), but end close to the center of the Smith chart for infinite frequency (the diode model itself will be RS), and we see the 50 Ohms of the opposite NWA port.
-> With CA0 and CC0 present, and no resistors in series with CA0 and CC0, the end-point for infinite frequency would be at zero Ohm (the very left in the Smith Chart).

DC-Off Spar Modeling: vD=-2V

A Closer Look at the Diode Anode-Cathode Capacitor



CAC was modeled in the CV-modeling section, at 1MHz.
Therefore, the model matches well the low frequencies.

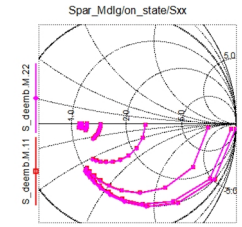
However, the CAC curve above, obtained from S-pars,
exhibits an increase of capacitance vs. freq.
This is an indicatation for the presence of a series inductor.

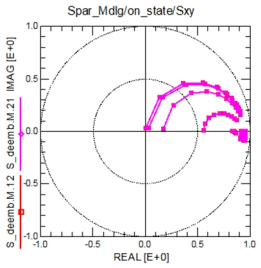
SisConsult

-30-

DC-On Spar Modeling

S-Parameter DC-ON Modeling





- the diode **Transit Time** will be modeled
- the already assumed **Series Inductor** will become pretty evident and will be modeled too.

SiConsult

A Quick Intermezzo:

DC-On Spar Modeling

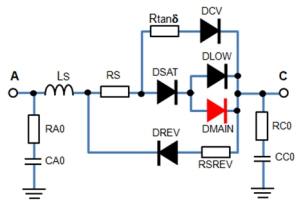
The Influence of the Diode Transit Time TT to the CV Curve

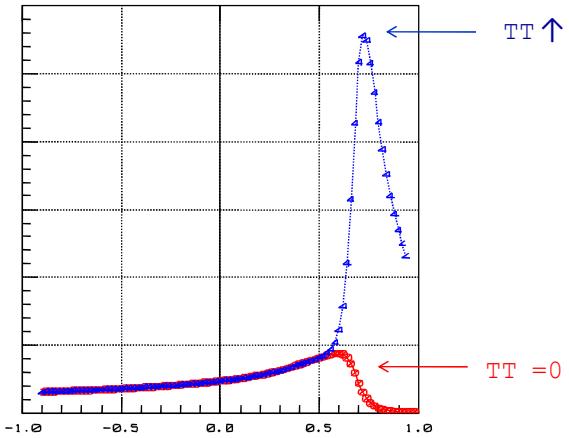
Transit Time affects the Diffusion Capacitance:

$$C_D = T_T * g_D$$

with

$$g_D = \frac{\partial i_D}{\partial v_D}$$



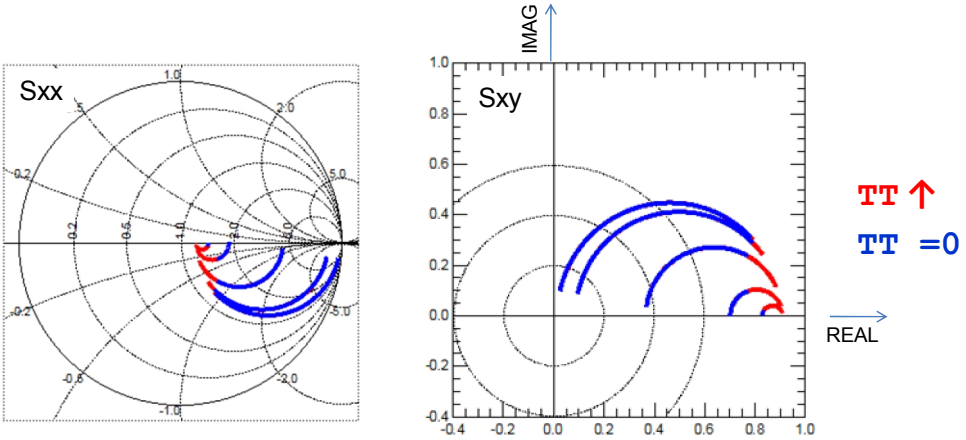


Note: due to its dependency on the diode conductance gD, apply the TT parameter of the MAIN DC diode

SiConsult

Note:
The plot above is obtained from an S-parameter simulation, converted to CV. The additional 'explosion' of the CV curve at diode threshold, due to the transit time TT, multiplied by 'exploding' diode conductivity gD, is clearly visible. The collapsing total capacitance towards further forward biasing is due to the shortening of Space Charge and Diffusion Capacitance by the internal diode ON-state resistance (~0 Ω).

The Transit Time Parameter Effect in the Diode S-Parameters Plots

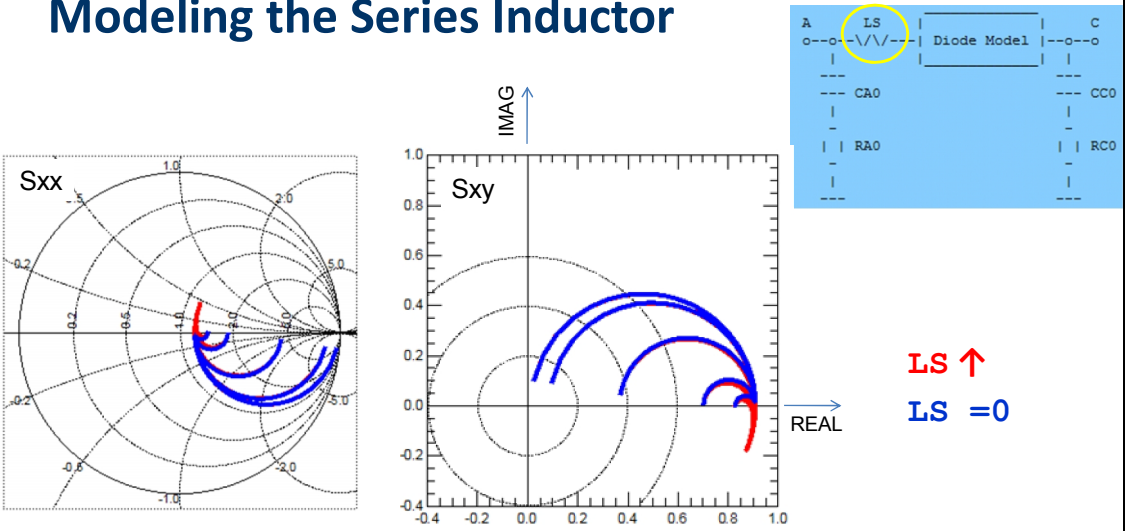


The Transit Time Parameter TT adds phase to the Sxx and Sxy traces.

For modeling TT, the best DC biasing is equal to the threshold voltage of the diode, typically ~0.7V

Note: for TT -> infinite, the end point of the Sxx and Sxy traces will be the x-axis in both, the Smith and Polar plot.

Modeling the Series Inductor



The series inductor lets Sxx and Sxy trespass the x-axis in both, the Smith and the Polar Plot

Back to Top

Nonlinear-RF Inspection

Outline

- Introduction
- Modeling Steps
  - DC Forward
  - DC Reverse
  - CV Modeling
  - S-Parameter
- **Nonlinear-RF Inspection**
- Time-Domain Inspection
- Modeling Result

35

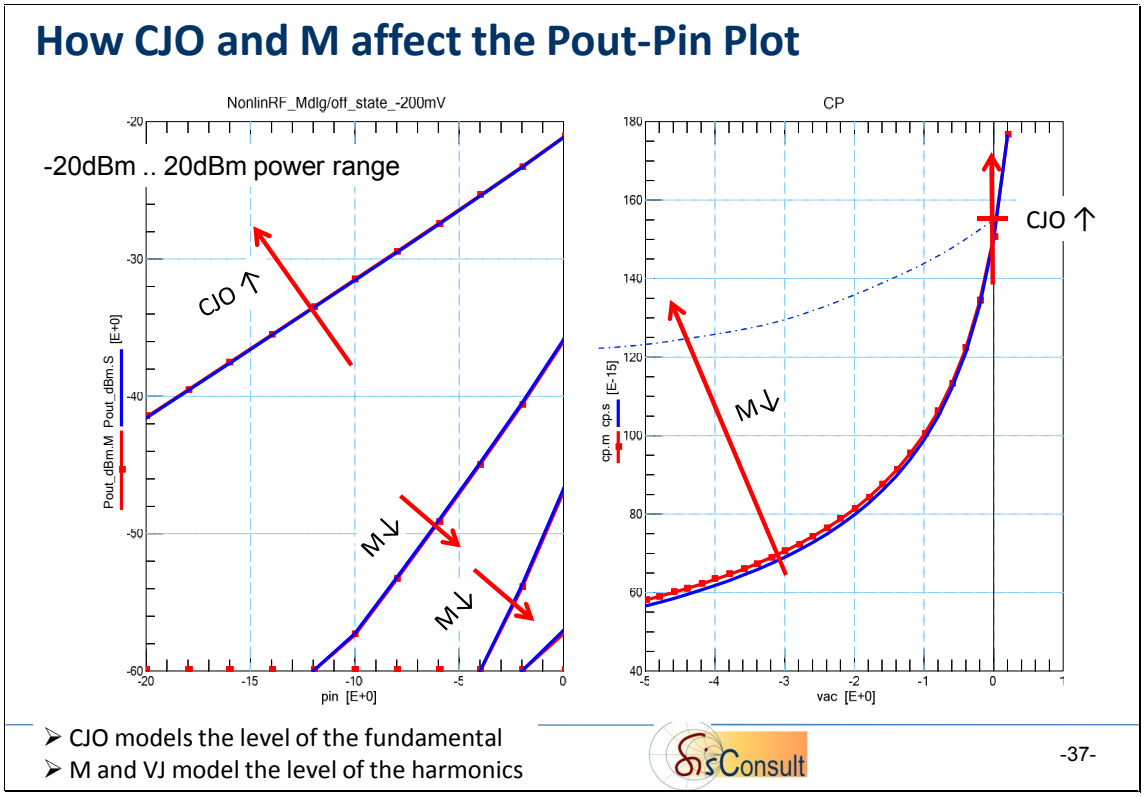
Nonlinear-RF
Pout vs. Pin for DC OFF State

- In the diode's OFF state,
  the capacitive conductance dominates.

  Therefore, the CV parameters CJO, M and VJ
  can also be obtained from nonlinear-RF measurements.

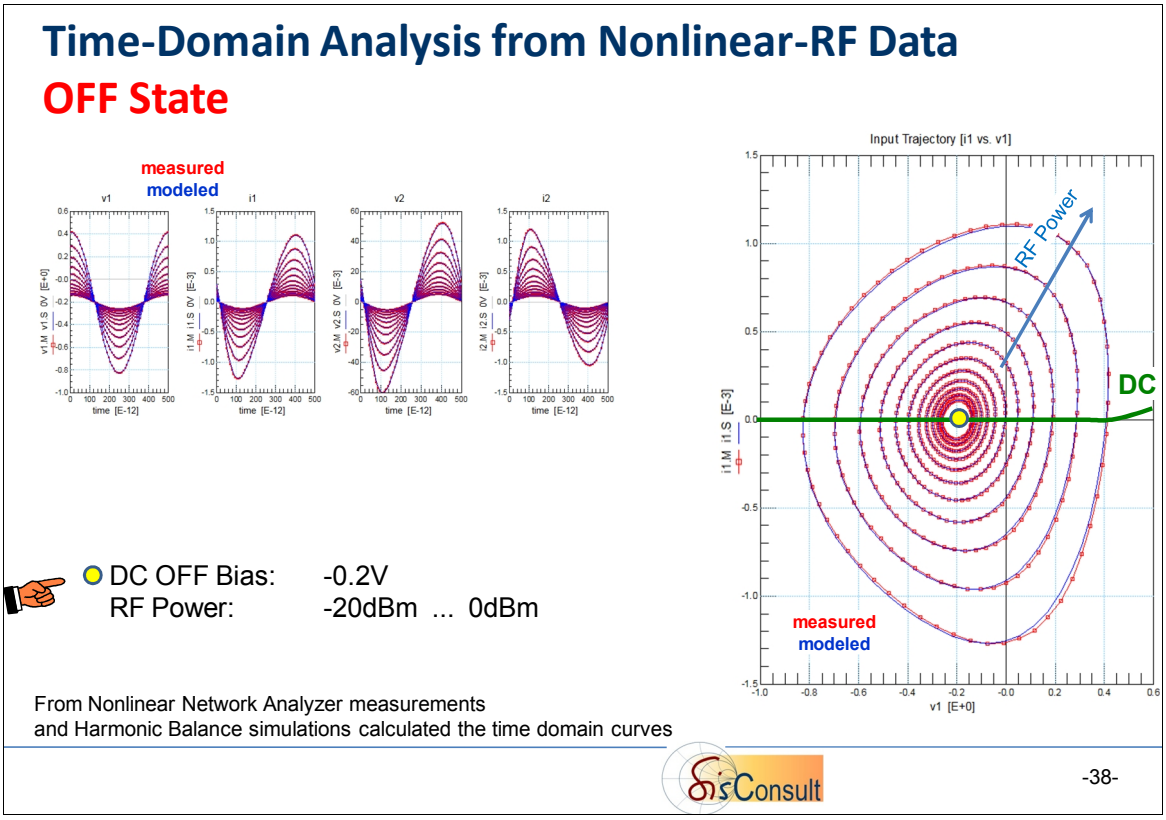
- Additionally, Nonlinear-RF data can be converted into time domain signals,
  what gives important insights into the *real* model behavior.

-36-



Note: the lower the parameter M becomes, the flatter, i.e. the more linear, the CV trace becomes.

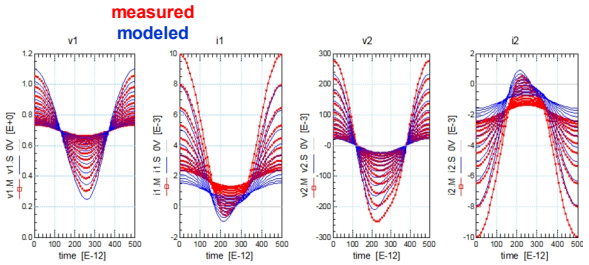
-> A more linear characteristic means less harmonics: the distance between fundamental and harmonics increases.



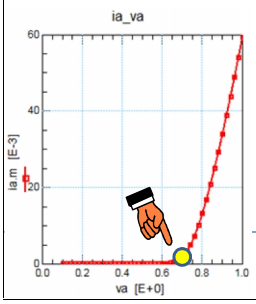
Note: in the Input Trajectory (iD vs vd), above on the right, watch how far the increasing RF signal can rotate around the DC bias point and extend into the beginning ON state of the diode.

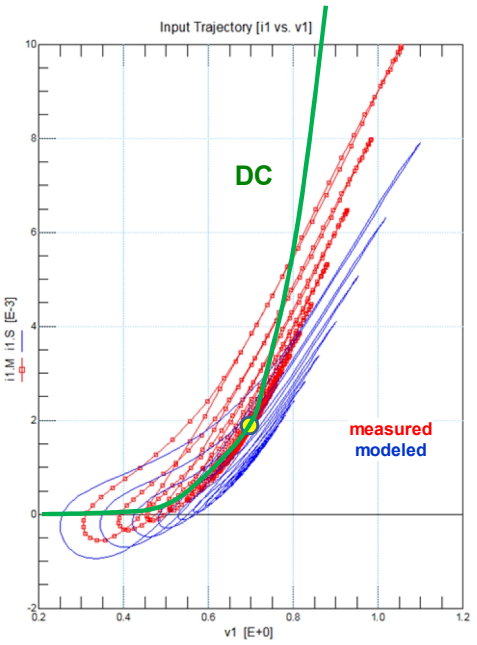
Time-Domain Analysis from Nonlinear-RF Data

Threshold to ON State



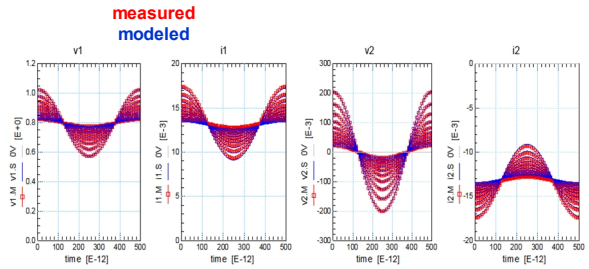
- DC ON Bias: 0.7V (threshold)
  RF Power: -20dBm ... 0dBm



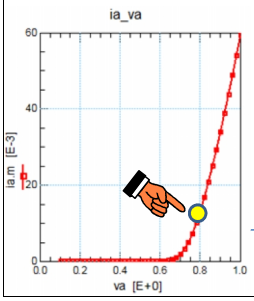


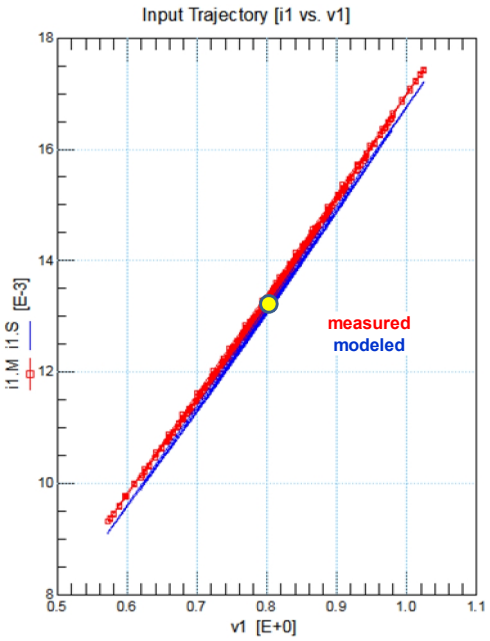
Time-Domain Analysis from Nonlinear-RF Data

ON State



- DC ON Bias: 0.8V (threshold)
  RF Power: -20dBm ... 0dBm





Back to Top

Time-Domain Inspection

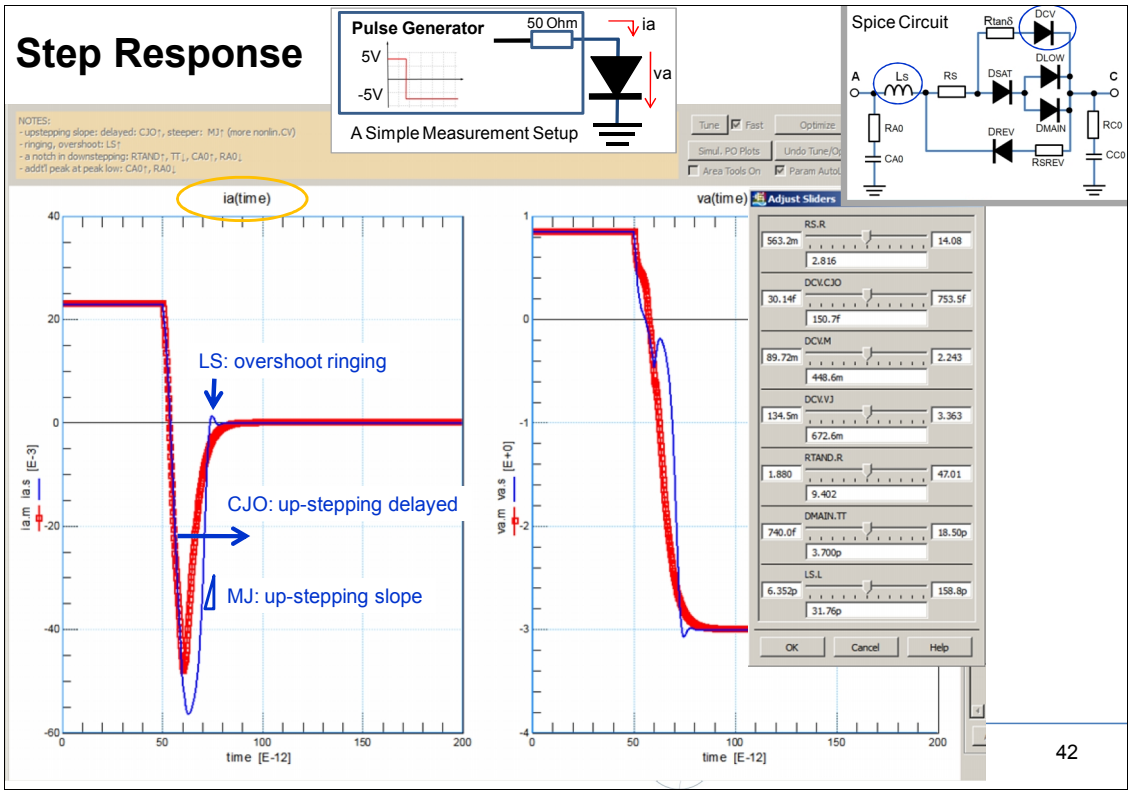
Outline

- Introduction
- Modeling Steps
  - DC Forward
  - DC Reverse
  - CV Modeling
  - S-Parameter
- Nonlinear-RF Inspection
- **Time-Domain Inspection**
- Modeling Result

SisConsult

41

Step Response



42

Back to Top

Modeling Result

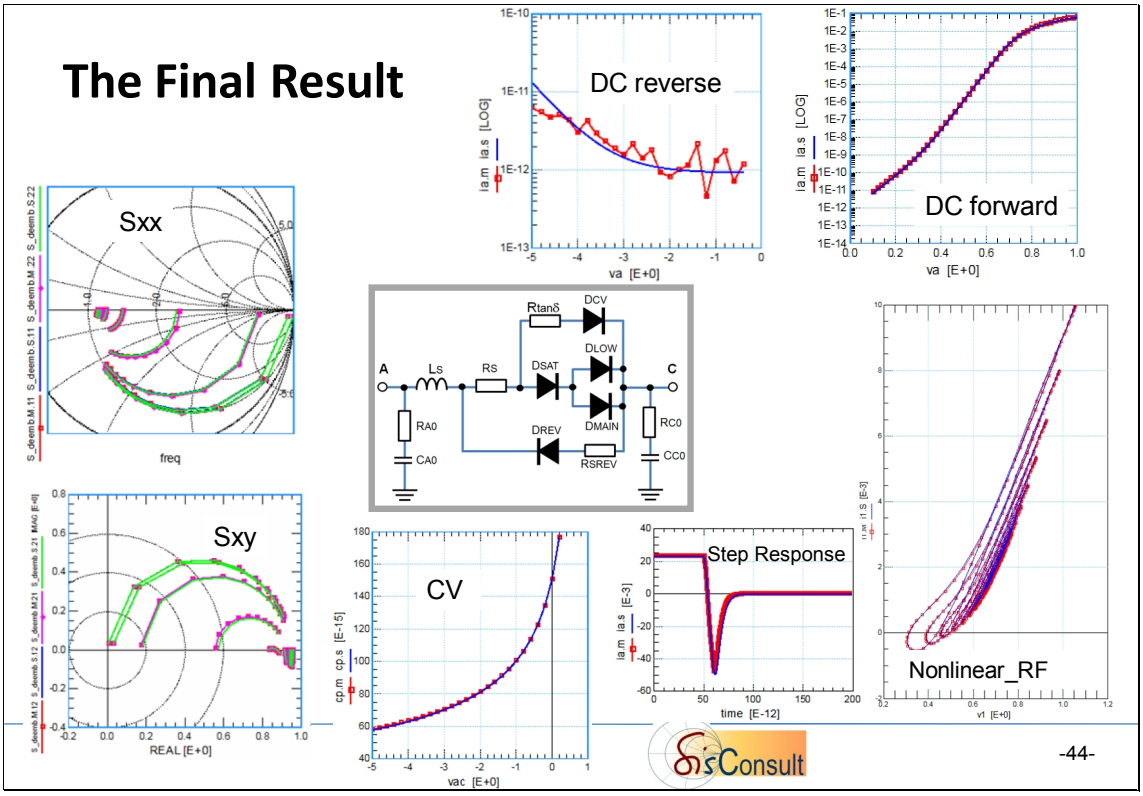
Outline

- Introduction
- Modeling Steps
  - DC Forward
  - DC Reverse
  - CV Modeling
  - S-Parameter
- Nonlinear-RF Inspection
- Time-Domain Inspection
- **Modeling Result**

SiConsult

43

The Final Result

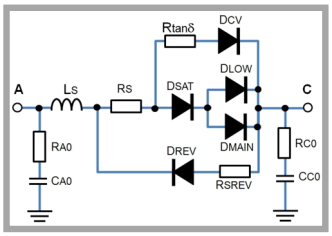


SiConsult

-44-

Spice Netlist

```
.SUBCKT Diode_Modeling  A=1  C=2

LS.L 1 11 2.868E-011

*---forward DC modeling
RS.R    11  111  2.927
DSAT   111   12  DSAT
DMAIN   12    2  DMAIN
DLOW    12    2  DLOW

*---reverse DC modeling
RSREV.R  2   21  2.5E+007
DREV    21   11  DREV

*---CV modeling
RTAND.R  111  121  1.2
DCV      121    2  DCV

*---parasitic Cs and Rs
CA0.C      1   10  8.511E-015
RA0.R     10    0  33.76
CC0.C      2   20  9.903E-015
RC0.R     20    0  16.79

*---model cards
.MODEL DLOW  D  IS=9.235E-13  N=1.829   CJO=1E-18
.MODEL DMAIN D  IS=3.007E-15  N=0.9797  CJO=1E-18     BV=10   IBV=1E-6   TT=3.314E-12
.MODEL DSAT  D  IS=0.004002   N=0.536   CJO=1E-18
.MODEL DREV  D  IS=4.378E-15  N=24.31   CJO=1E-18
.MODEL DCV   D  IS=1E-25      N=2       CJO=1.51E-13  M=0.452  VJ=0.675  FC=0.5

.ENDS
```



SisConsult

-45-

SisConsult
Ingenieurbüro - Engineering Office

Dr.-Ing. Franz Sischka

Consulting Services
for Electronic Device
Measurements,
Data Verification
and Modeling

www.SisConsult.de

eMail: franz.sischka@SisConsult.de

-46-

Back to Top